# Polycides, Salicides and Metals Gates

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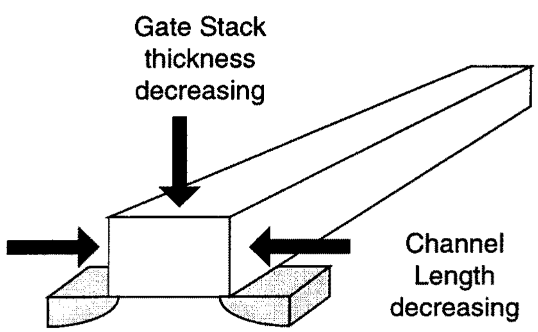
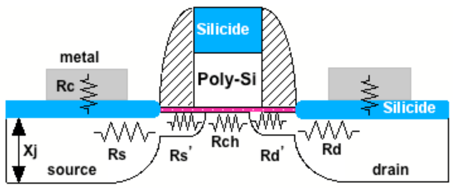
# MOS Gate Electrode



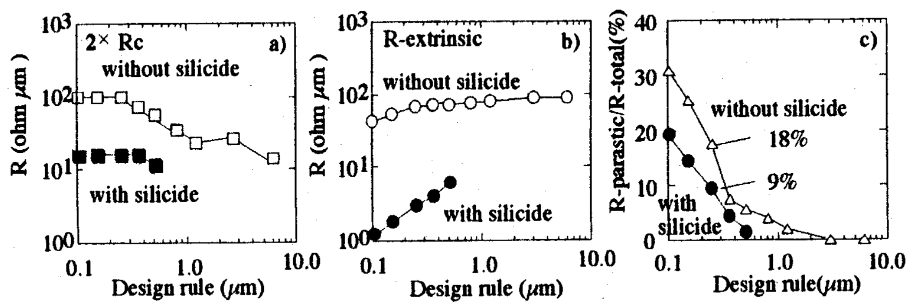

- Gate electrode is also used as an interconnect layer in many applications.
- As channel length is scaled, gate resistance increases.

# Effect of Scaling of Contacts and Junctions




R (total) = Rch + Rparasitic
Rparasitic = Rextension + Rextrinsic
Rextension = Rd' + Rs'
Rextrinsic = Rd + Rs + 2Rc

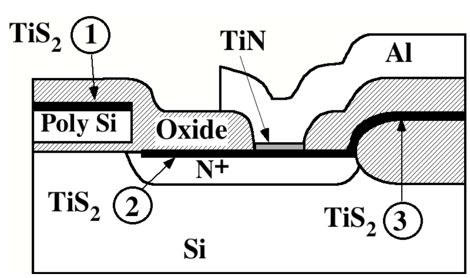
Ref: Ohguro, et al., ULSI Science and Technology 1997, Electrochemical Soc. Proc., Vol. 97-3




Silicidation of junctions is necessary to minimize the impact of junction parasitic resistance



# Silicides as Local Interconnect




To minimize parasitic resistance we use:

1. Polycide gate (silicide on polysilicon)
2. Salicide (self aligned silicide) on source-drain
3. Local interconnection

# Why use silicides?

- Low resistance
- Good process compatibility with Si
- Little or no electromigration
- Easy to dry etch
- Good contacts to other materials.

But these are many problems in integrating silicides in an IC as we will see later in this chapter.

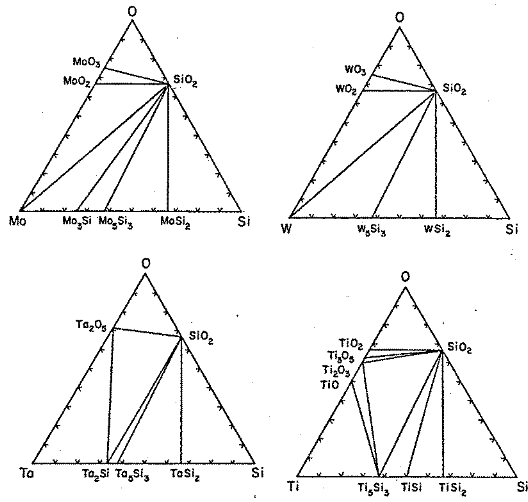


# Advanced Salicide Technologies

| Silicide | Thin film resistivity (μΩcm) | Sintering temp (˚C) | Stable on Si up to (˚C) | Reaction with Al at (˚C) | nm of Si consumed per nm of metal | nm of resulting silicide per nm of metal | Barrier height to n-Si (eV) |
|---|---|---|---|---|---|---|---|
| PtSi | 28-35 | 250-400 | ~750 | 250 | 1.12 | 1.97 | 0.84 |
| $TiSi_2$ (C54) | 13-16 | 700-900 | ~900 | 450 | 2.27 | 2.51 | 0.58 |
| $TiSi_2$ (C49) | 60-70 | 500-700 | | | 2.27 | 2.51 | |
| $Co_2Si$ | ~70 | 300-500 | | | 0.91 | 1.47 | |
| CoSi | 100-150 | 400-600 | | | 1.82 | 2.02 | |
| $CoSi_2$ | 14-20 | 600-800 | ~950 | 400 | 3.64 | 3.52 | 0.65 |
| NiSi | 14-20 | 400-600 | ~650 | | 1.83 | 2.34 | |
| $NiSi_2$ | 40-50 | 600-800 | | | 3.65 | 3.63 | 0.66 |
| $WSi_2$ | 30-70 | 1000 | ~1000 | 500 | 2.53 | 2.58 | 0.67 |
| $MoSi_2$ | 40-100 | 800-1000 | ~1000 | 500 | 2.56 | 2.59 | 0.64 |
| $TaSi_2$ | 35-55 | 800-1000 | ~1000 | 500 | 2.21 | 2.41 | 0.59 |

- **$TiSi_2$ has high thermal budget as the low resistance phase requires T > 800°C**
- **$TiSi_2$ and $CoSi_2$ have high Si consumption ⇒ problem in scaling junctions**
- **NiSi has lower Si consumption**
- **$WSi_2$ can be deposited by CVD ⇒ ease in manufacturing**

# Ternary Phase Diagrams



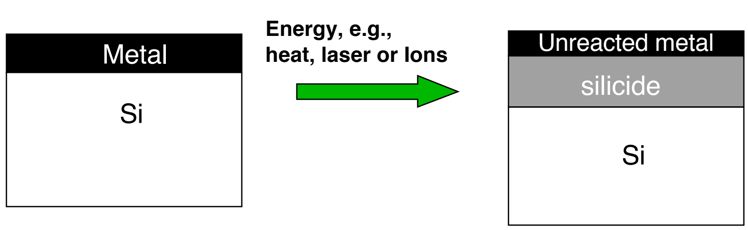

- Ternary Phase Diagrams are good indicators of stability.
- Existance of a ***tie line*** indicates that the system is stable.



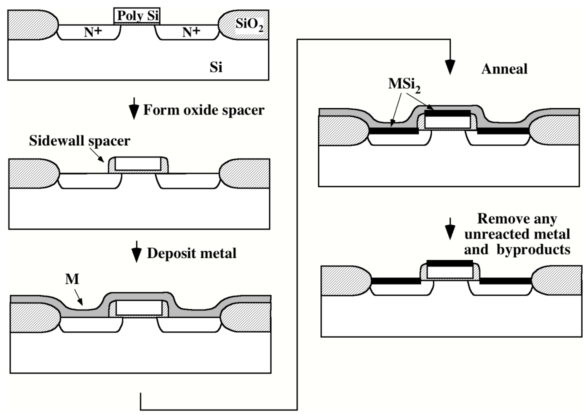
# Silicide Formation Techniques

**Metal deposition on Si and formation by thermal heating, laser irradiation or Ion beam mixing.**

- **Sensitive to interface cleanliness and heavy doping**
- **Selective silicidation on Si possible**
- **Widely used for silicides of Pt, Pd, Co, Ti and Ni**
- **Can't be used for W, Mo and Ta**



# Salicide (self-aligned silicide) process

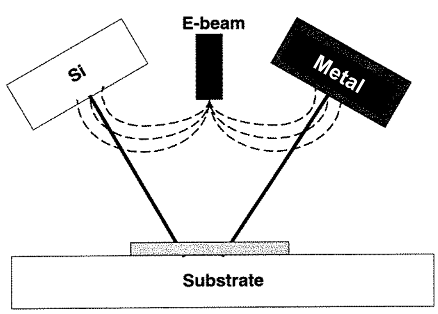



**Simultaneous silicidation of polysilicon gate, source and drain regions.**



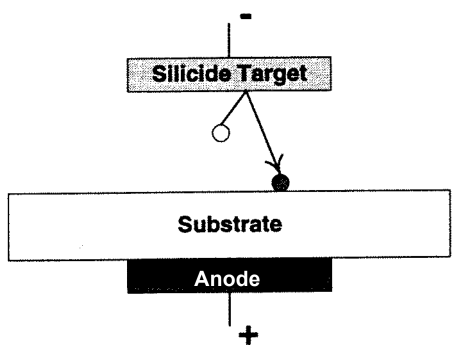
# Co-evaporation (E-gun) of metal and Si

- Poor process control
- Poor step coverage
- Good tool for research but not used in manufacturing



# Sputtering from a composite target

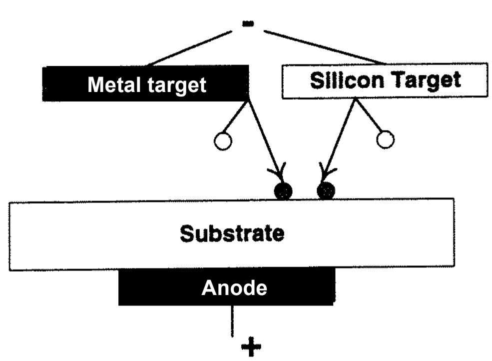
- Possibility of high level of contaminants (C,O, Na, Ar)
- Poor step coverage
- Used for $MoSi_2$ and $WSi_2$





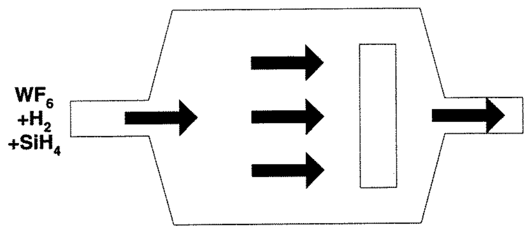

# Cosputtering from two targets of metal and Si

- Poor step coverage
- Questionable process control
- Good tool for research but not used in manufacturing



# Chemical Vapor Deposition (CVD)

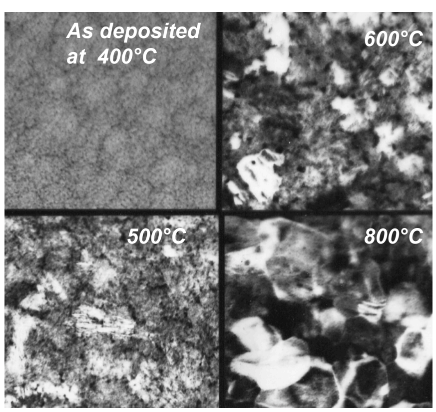
- Good process control for manufacturability
- Clean microcrystalline films with excellent step coverage
- Available for only $WSi_2$






# Thermal processing

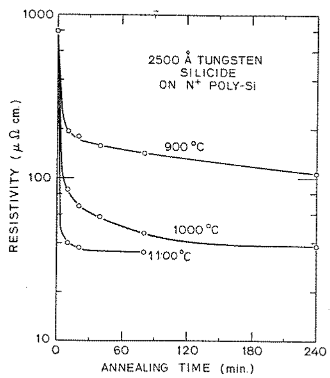
*TEM of CVD $WSi_2$*



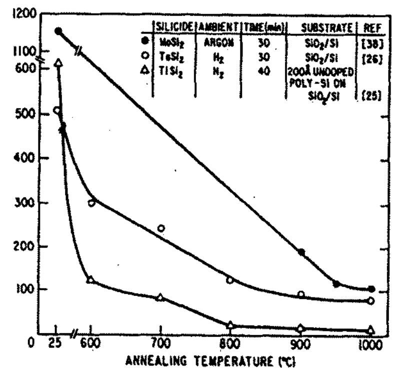

- As deposited films are amorphous or microcrystalline
- Upon annealing grains grow
- Higher temperature and longer time give bigger grains
- Possible phase change

Ref: K. C. Saraswat, et al., IEEE TED., November, 1983.

# Effect of Annealing on Resistivity




Ref: K. C. Saraswat, et al., IEEE TED., Nov., 1983.



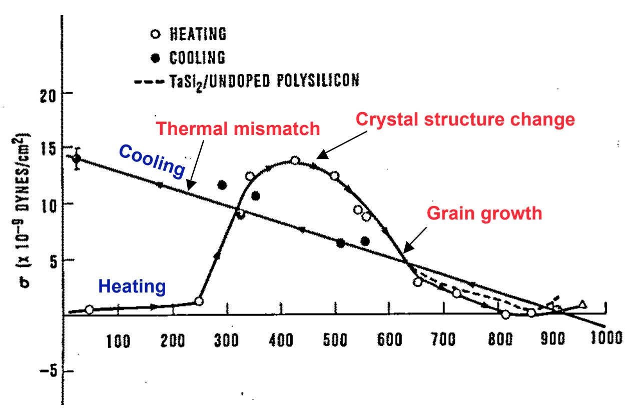

Ref: P. Chow, IEEE Trans. Electron. Dev., 1983).

- As deposited films have high resistivity
- Upon annealing resistivity decreases
- Higher temperature and longer time give lower resistivity

  ⇒ correlation with grain growth

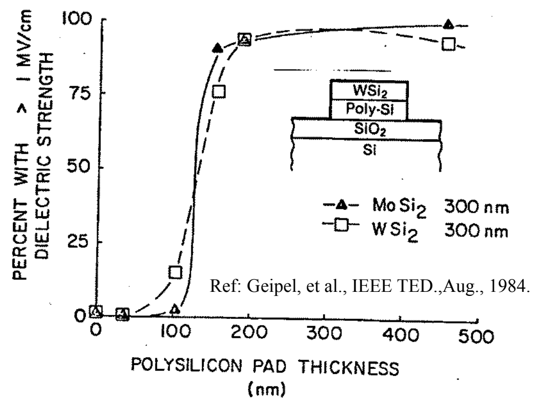


# Stress in Silicides




- Internal stress controlled by deposition parameters
- Difference in thermal expansion rates of Si and silicide
- Contaminants in silicide
- Structure and composition of the silicide film

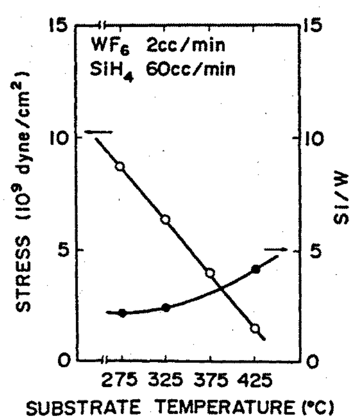
# Stress in Silicides

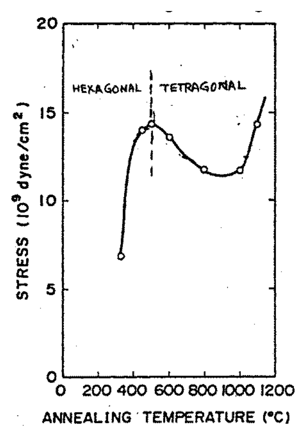



- Excessive stress in polycide gates can cause gate shorts, cracks, lifting
- Generally need a buffer layer of poly-Si to maintain reliability
- Or use other methods to minimize stress



# Effect of structure and Composition on Stress in Silicides

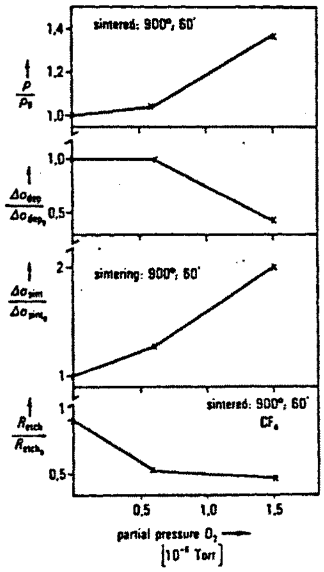



- Stress can be minimized by making Si rich silicide films
- Stress can be generated due to structural changes

# Effect of Contaminants

**Effect of oxygen contamination on the properties of $TaSi_2$ films**




**Resistivity**

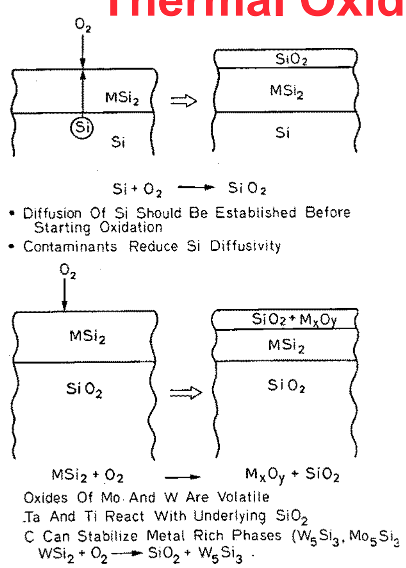
**Stress after deposition**

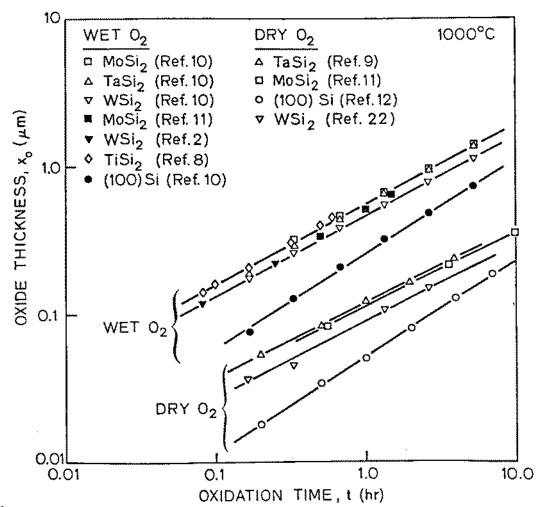
**Stres after anneal**

**Etch rate variation due to stress**



# Thermal Oxidation of Silicides

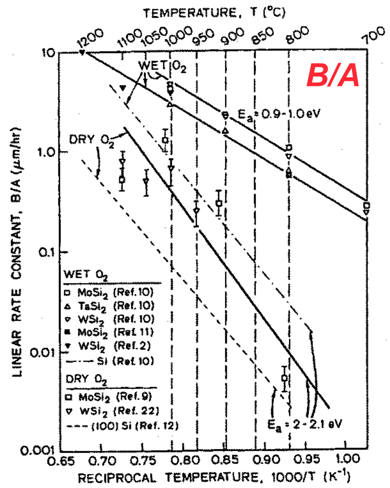


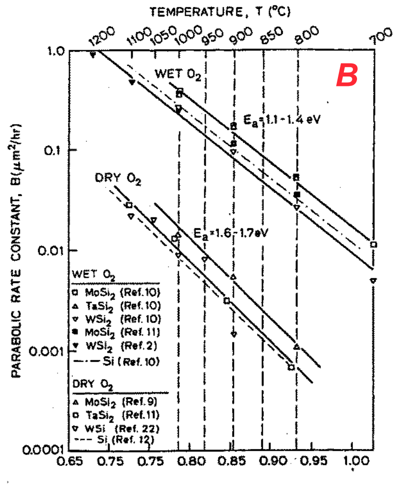




- ***Need excess Si for proper thermal oxidation***
- ***All silicides show similar oxidation rates***
- ***Silicides oxidize faster tha Si***

Lie, Tiller and Saraswat, Journal of Appl. Phys., Vol. 56 (7), Oct., 1984.

# Oxidation Rate Constants



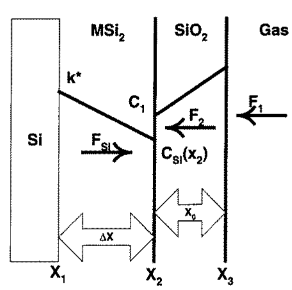

$$\frac{X_0^2}{B} + \frac{X_0}{B/A} = t + \tau$$

*Parabolic rate constant B is about the same as for Si*
*Linear rate constant B/A is much higher than for Si*

Lie, Tiller and Saraswat, Journal of Appl. Phys., Vol. 56 (7), Oct., 1984.



# Oxidation Kinetics




$$\frac{X_0^2}{B} + \frac{X_0}{B/A} = t + \tau$$

$$B = 2 \cdot C^* \cdot D_{ox}/N_1$$

$$B/A = \frac{C^*}{N_1} \cdot \frac{1}{\left\{\frac{1}{h} + \frac{C^* \cdot \Delta x}{k^* \cdot D_{Si}} + \frac{1}{k_1 \cdot k^*}\right.}$$

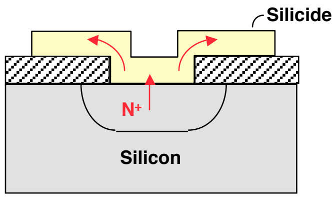
If $D_{Si}$ is large, then this reduces to:

$$B/A = \frac{C^* \cdot k_1 \cdot k^*}{N_1}$$

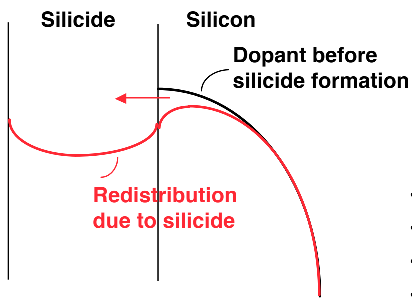
**k* is partition coefficient of Si between Si and $MSi_2$**
**C* is concentration of oxidant in $SiO_2$**
**$C_0$ is concentration of oxidant at $SiO_2$ surface**
**$D_{ox}$ is diffusivity of oxidant in $SiO_2$ = 5E-10 cm$^2$/sec for $H_2O$ and 5E-9 cm$^2$/sec for $O_2$**
**$D_{si}$ is diffusivity of Si and $MSi_2$ = 1E-7 cm$^2$/sec.**

- ⇒ *$D_{si}$ is much higher than $D_{ox}$*
- ⇒ *Rate limiting step is diffusivity of oxidant in $SiO_2$. Therefore $B_{si} = B_{silicide}$*
- ⇒ *B/A is much higher for silicides because it is easier to break a Si bond at the silicide/Si interface than at the Si/Si interface (higher k*)*

# Dopant Redistribution in Silicide/Silicon




| Year | Junction Depth ($\mu$m) |
|---|---|
| 1975 | 1.0 |
| 1985 | 0.5 |
| 1995 | 0.15 |
| 2005 | 0.05 |
| 2010 | 0.015 |




**Specific contact resistivity**

$$\rho_c = \rho_{co} \exp\left( \frac{2\phi_B}{q\hbar} \sqrt{\frac{\varepsilon_s m^*}{N}} \right) \quad ohm - cm^2$$

Doping density (N)

**ISSUES**

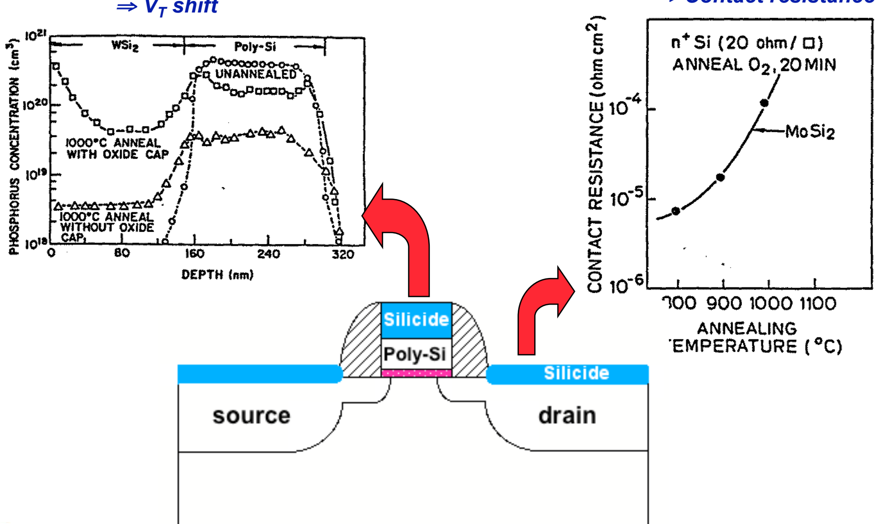
- Dopant diffusion in silicide and silicon
- Segregation at interfaces and grain boundaries
- Solubility in silicide and silicon
- Compund formation and precipitation



# Dopant Redistribution/Diffusion

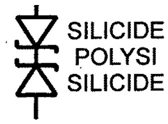
*Change in gate Fermi level*
*⇒ $V_T$ shift*

*Change in surface doping*
*⇒ Contact resistance*

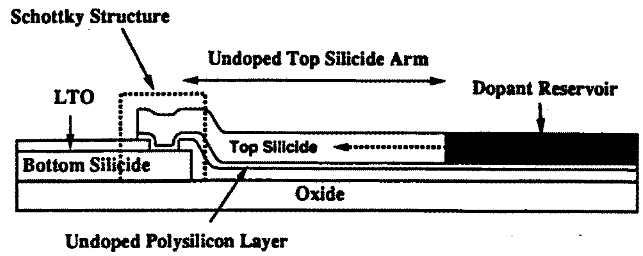


# Characterization of Dopant Diffusion

## Schottky Test Structure



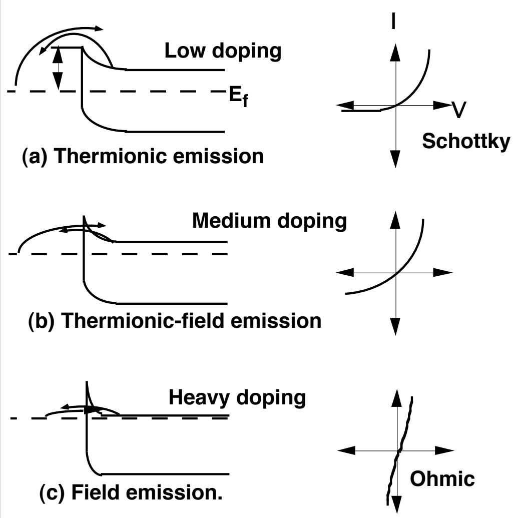

$$N(x,t) = N_o erfc\left(\frac{x}{2\sqrt{Dt}}\right)$$

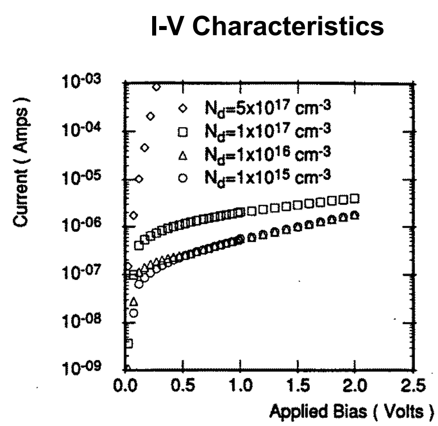



- Dopant Diffusion in silicides very rapid, vertical profiling not possible
- Lateral diffusion in a long thin film can be measured
- Vary arm length and estimate doping at the end of the arm by measuring I-V characteristics



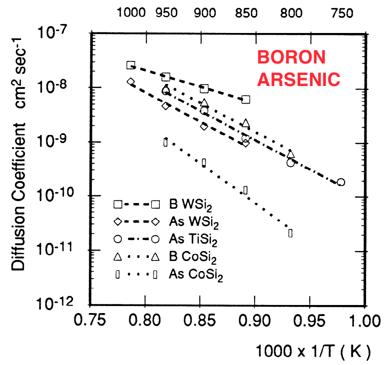
# I-V Characteritics of Si/Silicide

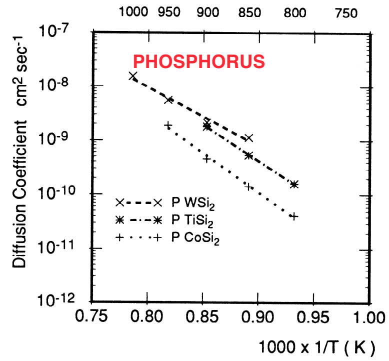



**Current in a Schottky contact is very sensitive to doping density**

# Dopant Diffusion in Polycrystalline Silicides




**Dopants diffusion in polycrystalline silicides is:**

- **5 - 6 orders of magnitude higher than in single crystal silicon**
- **3 - 4 orders of magnitude higher than in polycrystalline silicon**

**PROBLEMS:**

**$N^+/P^+$ spacing**

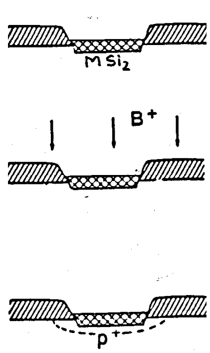
**Contact resistance can change**

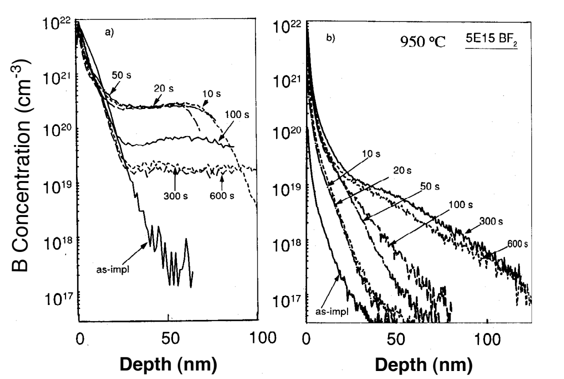
**$V_T$ shift can occur in a polycide**

Chu, Saraswat and Wong
IEEE Trans. Electron Dev., October 1992,



# Solid Source Diffusion from Silicides



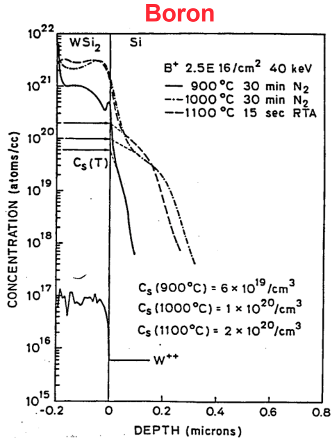

In $COSi_2$ In Si after silicide removal

Boron profiles after diffusion at 950°C of 50 nm $COSi_2$ implanted with 5 X $10^{15}$ $cm^{-2}$ $BF_2$ (a) and (b)in Si after silicide removal.

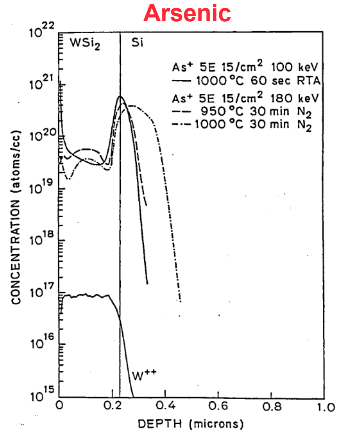
- **No ion-implantation damage in Si**
- **Ultra-shallow junction possible**
- **High leakage if metal gets into Si**

# Solid Source Diffusion from Silicides

**Boron**




**Arsenic**



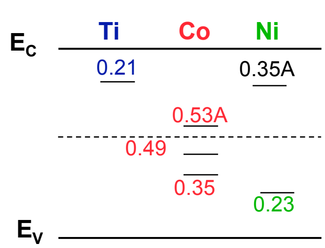

Boron and arsenic profiles after diffusion from $WSi_2$

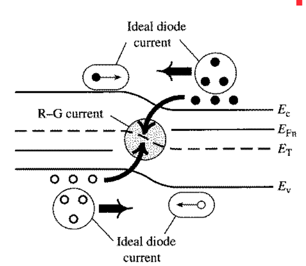
Shone, Saraswat and Plummer, IEEE Int. Electron Device Meeting, 1985



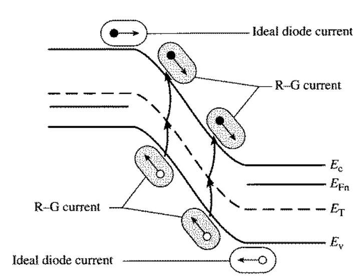
# P-N Junction Currents Modified Due to Traps

**Energy levels in Si bandgap due to metals contaminants**




**Forward Biased P-N Junction**




**Reverse Biased P-N Junction**

- **The total diode current is given by:**
  $I = I_{DIFF} + I_{R\text{-}G}$
- **Presence of metal in Si increases $I_{R\text{-}G}$**
- **Care must be taken to ensure that metal atoms don't diffuse in the depletion region**
- **Ensure minimum Si consumption**

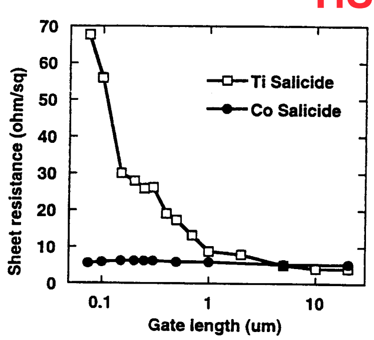
## Problem with Salicide Technology: Si Consumption in Silicide Formation

| Silicide | Si consumed per nm of metal (nm) | Resulting silicide per nm of metal (nm) |
|---|---|---|
| $TiSi_2$ (C54) | 2.27 | 2.51 |
| $CoSi_2$ | 3.64 | 3.52 |
| NiSi | 1.83 | 2.34 |

- **$TiSi_2$ and $CoSi_2$ consume excessive Si during formation**
  **⇒ Not scalable to ultrashallow junctions**
- **NiSi better suited for ultrashallow junctions**



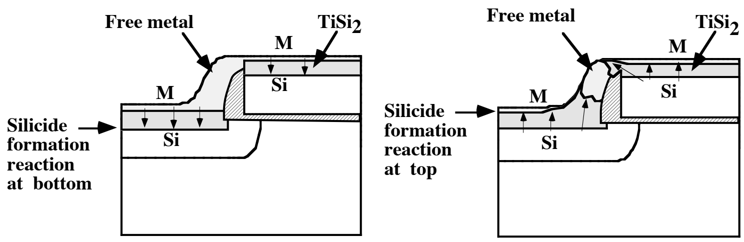
## Problem with Salicide Technology: $TiSi_2$ Scalability




| Silicide | Thin film resistivity (μΩcm) | Si consumed per nm of metal (nm) |
|---|---|---|
| $TiSi_2$ (C54) | 13-16 | 2.27 |
| $TiSi_2$ (C49) | 60-70 | 2.27 |

- **$TiSi_2$ has high resistance in narrow lines**
  **⇒ C49 to C54 transformation impeded**
- **Agglomeration of $TiSi_2$ in narrow lines**
- **$CoSi_2$ and NiSi are scalable to smaller dimensions**

# Transport Mechanism in Silicide Formation



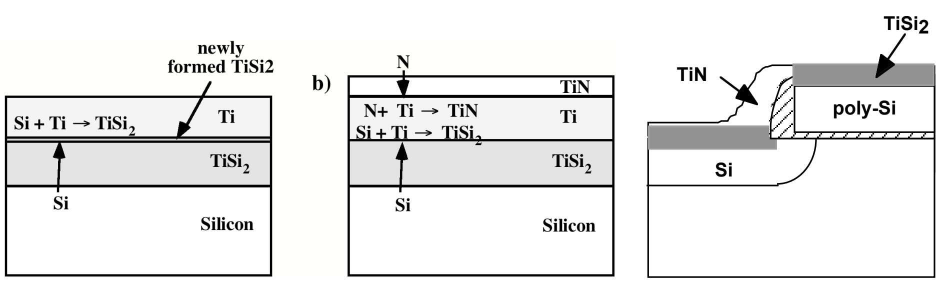

a) Metal diffuser
Pt
Pd
Ni
Co (low temperature)

b) Si diffuser
Ti
Ta
Co (high temperature)

- If silicon is dominant diffuser, lateral encroachment of the silicide over the oxide spacer can occur causing bridging.
- A barrier needs to be created over the spacer



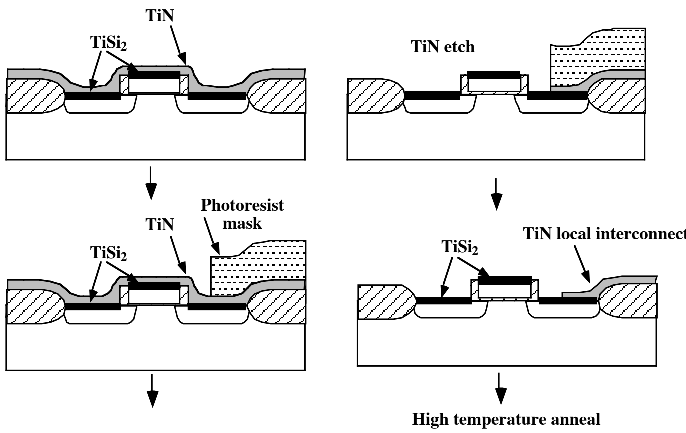
# How to Avoid Bridging?




- Anneal in an inert ambient or vacuum
- Only $TiSi_2$ formation

- Anneal in an ambient containing nitrogen
- Simultaneous formation of $TiSi_2$ and TiN
- TiN acts as a barrier to Si diffusion over the spacer

## Salicide process with TiN as a local interconnect




**Salicide process to obtain:**

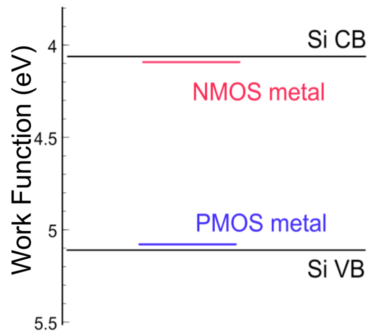
1. **$TiSi_2$ on top of polysilicon gate**
2. **$TiSi_2$ on top of source and drain**
3. **TiN as a local interconnect.**



## Direct Metal gate Electrode

- **Avoid**
  - **poly-Si depletion ⇒ increase in EOT**
  - **remote charge scattering ⇒ mobility degradation**
- **Suppress soft phonon scattering caused by softer metal-oxygen bond in high-K dielectrics**

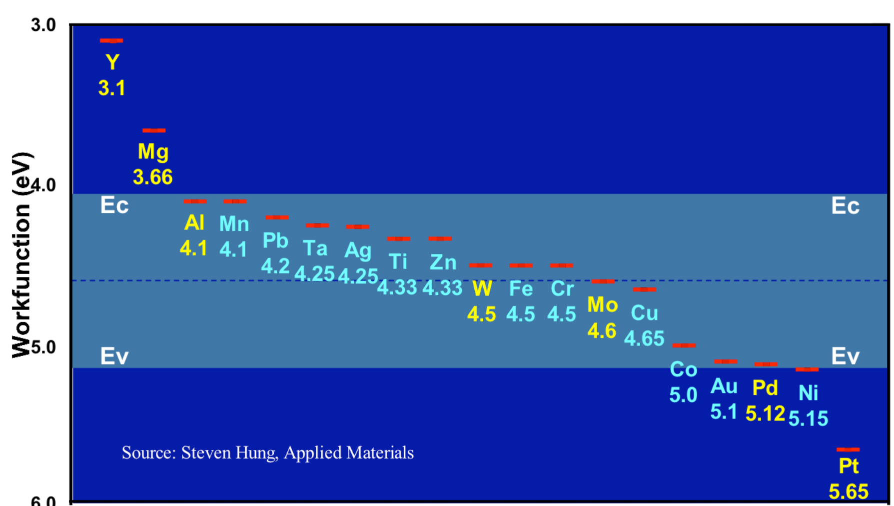
# Dual Metal gates - Choice of Metal




- **Adjust $V_T$ through gate electrode work function control**
  - **reduce ionized impurity scattering in channel**
  - **Need dual work function to adjust $V_T$**
- **We currently use $N^+$ poly-Si gate for NMOS and $P^+$ poly-Si for PMOS**
- **Choose metal with work function equal to Si band edge energies**



# Workfunction of Metallic Elements

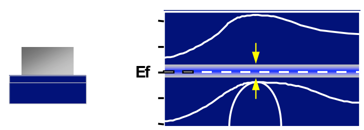



Source: Steven Hung, Applied Materials

- Many choices of metal work function available
- Are they practical?

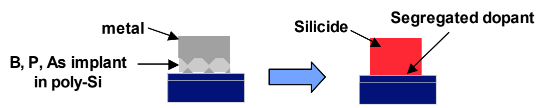
# Technologies for Gate Workfunction Engineering

• **SiGe alloy gate electrode:**



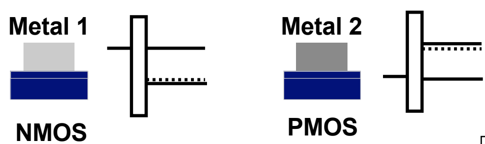

**Use Si & Ge alloying compositions to alter the band structure, and therefore the $E_f$.**

• **Fully silicide heavily implanted poly-Si gate electrode:**




**Form silicide on poly-Si by reacting with metal and fully consume Si. Use dopant segregation at the interface to control $E_f$**

• **Dual metallic gate:**

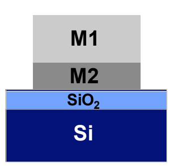


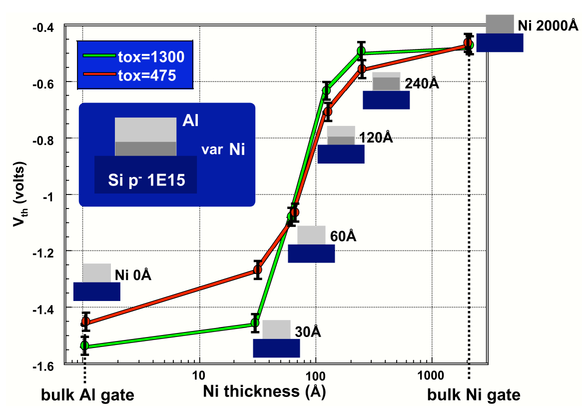

**Metal 1 and Metal 2 are individually selected for NMOS and PMOS, respectively.**

Source: Steven Hung, Applied Materials



# Sandwich Metal Electrode

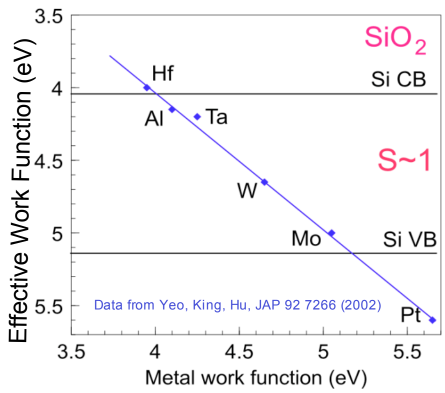



Ref: Steven Hung, Applied Materials

- **Choose M2 for workfunction adjustment and M1 for other considerations**
- **M1 and M2 should remain separated**
- **If alloyed then workfunction will change**

# $SiO_2$ Follows Ideal Schottky Model



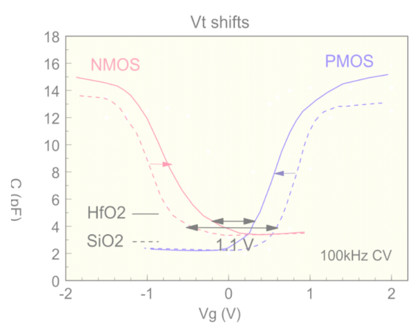

$$\Phi_{m,\mathrm{eff}} = \Phi_{m,\mathrm{vac}}$$

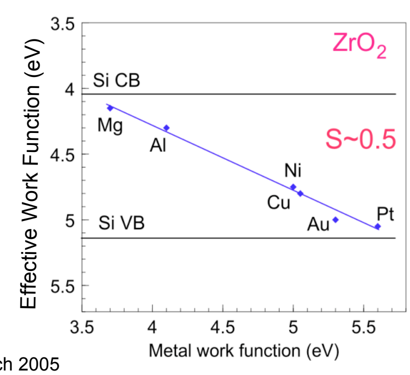
- **Poly-Si and metals on $SiO_2$ are like perfect Schottky**
- **Can use ideal band structure rules to construct band diagram and calculate work function**
- **But not on high K oxides**

Ref: Robertson, MRS March 2005



# $V_T$ shift problem with high K oxides



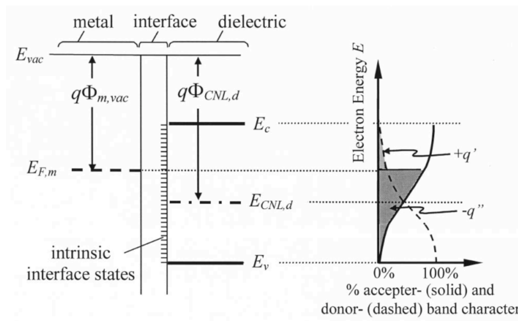




Ref: Robertson, MRS March 2005

- **$V_T$ shifts of poly-Si and metal gates on Hi K oxides, e.g. $HfO_2$, $ZrO_2$ compared to $SiO_2$ standard**
- **Poly-Si and metals on high-k dielectrics don't follow ideal Schottky model**
- **Can't use ideal band structure rules to construct band diagram and calculate work function**

# Energy band diagram and charging character of interface states for the metal-dielectric interface

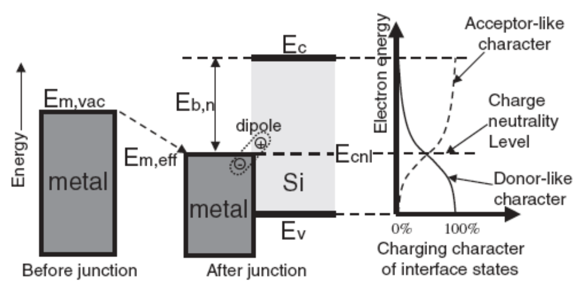
- Ideal Schottky model: when a metal and a semiconductor or a dielectric form an interface, there is no charge transfer across the interface
- A semiconductor or dielectric surface has gap states due to the broken surface bonds. These are spread across the energy gap.
- The wave functions of electrons in the metal tail or decay into the semiconductor in the energy range where the conduction band of the metal overlaps the semiconductor band gap. These resulting states in the forbidden gap are known as *metal-induced gap states* (MIGS) or simply *intrinsic states*.
- The energy level in the band gap at which the dominant character of the interface states changes from donorlike to acceptorlike is called the charge neutrality level $E_{CNL}$




Yeo, King, and Hu, J. Appl. Phys., 15 Dec. 2002

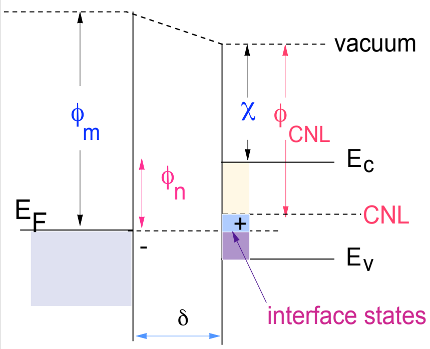


# Fermi Level Pinning




- Charge transfer occurs across the interface. Charging of the interface states creates a dipole that tends to drive the band lineup toward a position that would give zero dipole charge.
- This results in the metal work function getting pinned near the charge neutrality level $E_{CNL}$

# Band Alignments on oxides




- Schottky barrier height $\phi_n$ of metal on oxide depends on charge transfer at interface
- CNL aligns to metal $E_F$
- $\phi_n = S(\phi_m - \phi_{CNL}) + (\phi_{CNL} - \chi)$
- S is a dimensionless pinning factor given by

$$S = \frac{d\phi_n}{d\phi_m} = \frac{1}{1 + \frac{Ne^2\delta}{\varepsilon}}$$

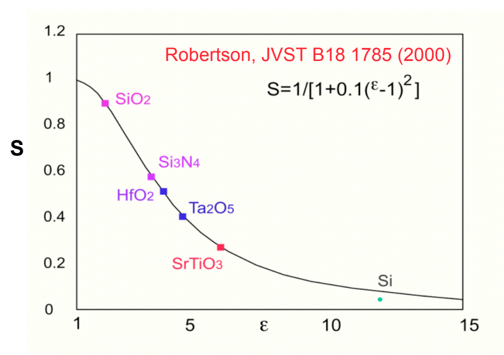
- ε is optical (electronic) portion of the dielectric constant
- No charge transfer, S=1 e.g. $SiO_2$
- Charge transfer, strong pinning, S=0

CNL = charge neutrality level of oxide,
N surface states/$m^3$/eV
δ = state decay length = dipole layer width

Robertson, JVST B18 1785 (2000)
Yeo, King, and Hu, J. Appl. Phys., 15 Dec. 2002

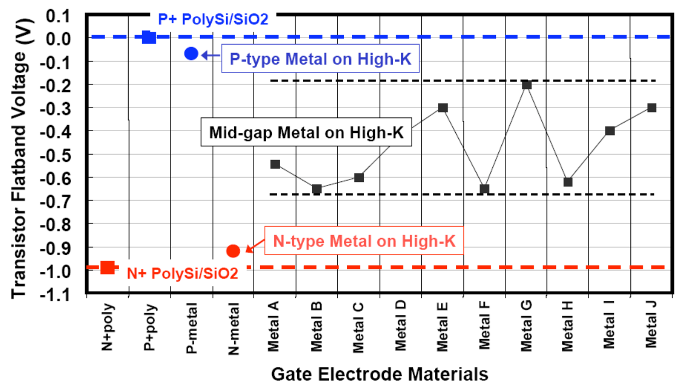


# Variation of the Schottky barrier *S* factor with electronic dielectric constant




- High K's are less 'Schottky-like' than $SiO_2$. Barrier heights change less than metal workfunction.
- People have found experimental tricks to obtain tunable workfunction

# Intel has dual metal-gate *C*MOS on $HfO_2$

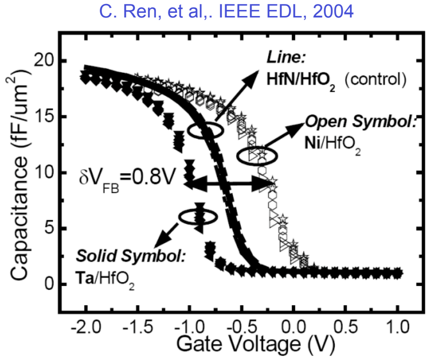



R Chau, IWGI, Tokyo 2003



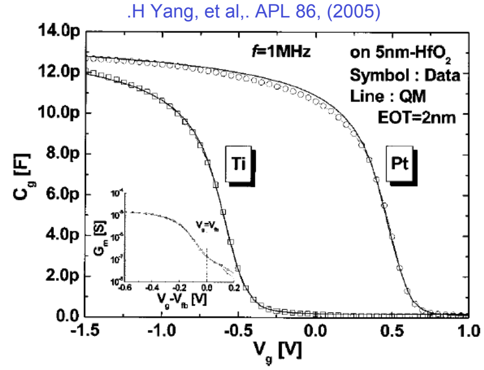
# Other evidence

C. Ren, et al,. IEEE EDL, 2004




0.8V split between hi-lo workfunctions

.H Yang, et al,. APL 86, (2005)




1.2V split between hi-lo metals